The Fir Filter Design and Analysis and Code Generation Using HDLCODER for Area and Power Efficient FPGA Implementation

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Abstract – Nowdays the digital signal processing is highly demanded as the competition amongst the different electronics companies is increasing to fulfill the demands of the consumers and hence the equalisers,filters need to be modified according to the requirements.Before dealing with the design of the filter we must analyse the filters this paper shows the analysis reports of different filters using FIR design in Filter design and Analysis tool (FDA) .DSP operation mainly include the Multiply and Accumulate MAC operation so we have designed RAM based FIR filter using HDLcoder in simulink where MAC is taken into the consideration.Also the Code generated by the HDL coder is implemented on the Xilinx ISE 14.7 .ISim vhdl simulator is used for simulation.The model is synthesized.RTL and Technology schematic is observed.

Index Terms – MATLAB,fdatool,HDLcoderFPGA,FIR

1. INTRODUCTION

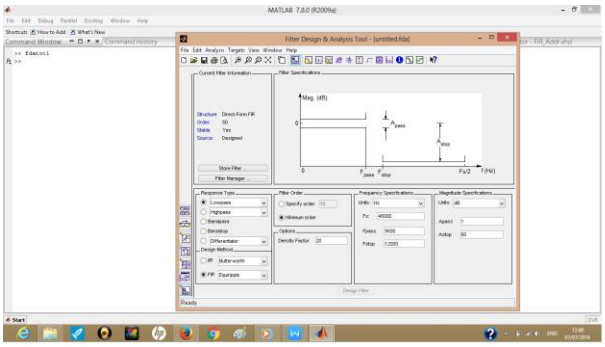
The filter designing has become basic requirement of any communication system or software radio or even the image and video-audio processing to achieve lossless systems.However, when dealing with the IIR filter or recursive filters we have to deal with the extreme unstable impulse response though its accuracy is high.The filter is implemented on SPARTAN 6 low power device.

2. PROPOSED WORK

As In signal processing, a finite impulse response (FIR) filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time. The impulse response of an Nth- order discrete-time FIR filter lasts for N + 1 samples, and then settles to zero[1]. A Finite impulse response (FIR) filter is a filter structure that can be used to implement almost any sort of frequency response digitally. An FIR filter is usually implemented by using a series of delays, multipliers and adders to create the filter output. Figure 1 shows the basic block diagram for an FIR filter of length N. The delays in operating on prior input samples. The hκ values are the coefficients used for multiplication, so that the output at time n is the summation of all the delayed samples multiplied by the appropriate coefficients. The processer selecting the filters length and coefficients is called as filter design. Dealing with MATLAB environment we have to consider some presumptions like to know about different tools integrated in it. As the FDAtool is used to analyse the implementation.No explicit multipliers are used in the design, this includes look-up tables (LUTs), shift registers, and a scaling accumulator for the computations.

3. SOFTWARE USED

To generate the filter code we used FDA tool HDLcoderof MATLAB And Xilinx ISE.14.7(64-bit)Xilinx Designing a digital filter in MATLAB and using HDL coder FIR filter code is generated and programming it onto an FPGA.MATLAB



fdatool is as shown in figure 1

Figure 1: MATLAB fdatool window

4. FLOW OF WORK

The filter coefficients obtained by quantising the filter using a "set quantization parameters"at the bottom left of the fdatool window.As we want RAM to be used in the FPGA implementation we must specify the quantization parameters as double precision floating point as the FPGA supports only floating point coefficients it is convinient to use the fdatool.

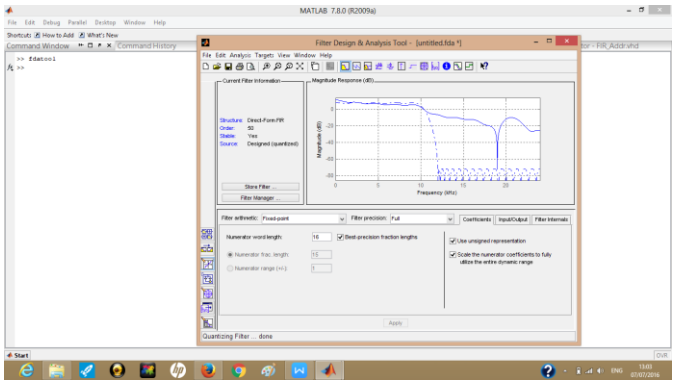


Figure 2:The quanitization Parameters

The RTL logic of The RAM based FIR is as shown in the figure below

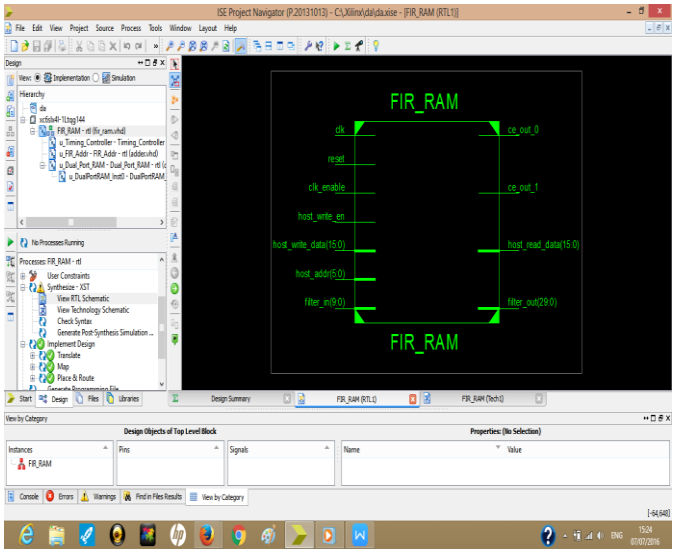


Figure 3:The top level entity

The RAM based Structure of FIR filter is designed using HDLcoder by giving a command "hdlcoderfirram.mdli" in

MATLAB command window we get the RAM based FIR filter and its associate blocks as shown in the figure 4.

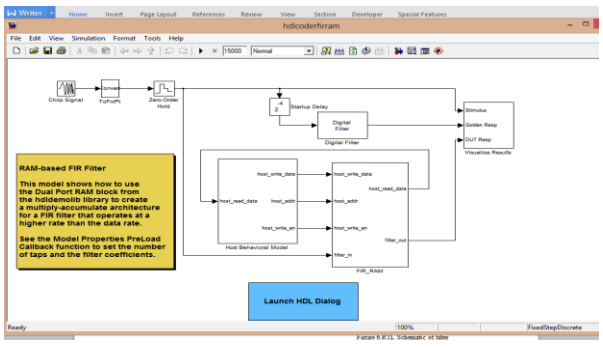


Figure 4.HDL coder dialog

After pressing the "LAUNCH HDL DIALOGUE"we get the following window in figure 5 where choose the code generation output as generate code and display generated model.Press "Generate" button to get the display as shown in figure 5

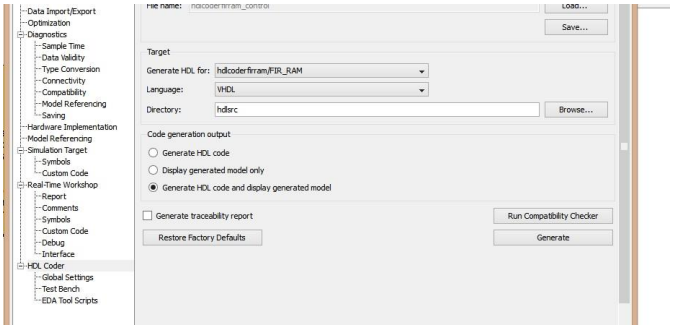


Figure 5:Configuration parameters

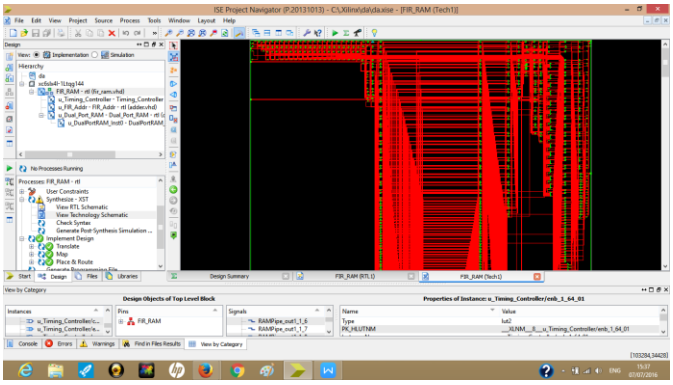


Figure 6:Technology schematic of Dual port RAM based FIR filter

The technology schematic is as shown in figurw It consists of LUTs describing Accumulator,FIR_RAM,Tapped delay.The design properties are shown in the figure the simulation tool is ISim and Package is TQG144 also the speed grade is -1L and the device it can be implemented on is XC6SLX4L.The Xilinx ISE environment is used to synthesize the code and implement the design.The device utilization summery i as shown in the table.

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	798	4,800	16%
Number of Slice LUTs	491	2,400	20%
Number used as logic	300	2,400	12%
Number used as Memory	32	1,200	2%
Number of occupied Slices	215	600	35%
Number of MUXCYs used	32	1,200	2%
Number of LUT Flip Flop pairs used	736		
Number of bonded IOBs	84	102	82%
Number of BUFG/BUFGMUXs	1	16	6%
Number of DSP48A1s	1	8	12%
Average Fanout of Non-Clock Nets	3.64		

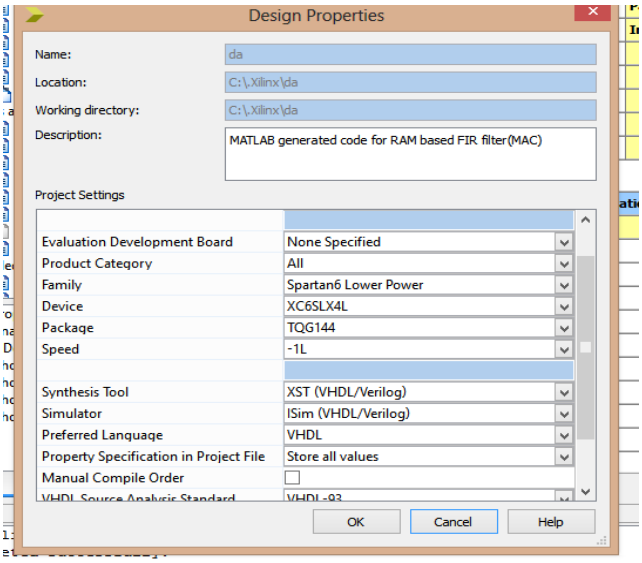


Figure 7:The design properties

The RTL schematic can show that the number of LUTs are more but the FPGA LUTs consumes less power as compared to the other DSP tools.

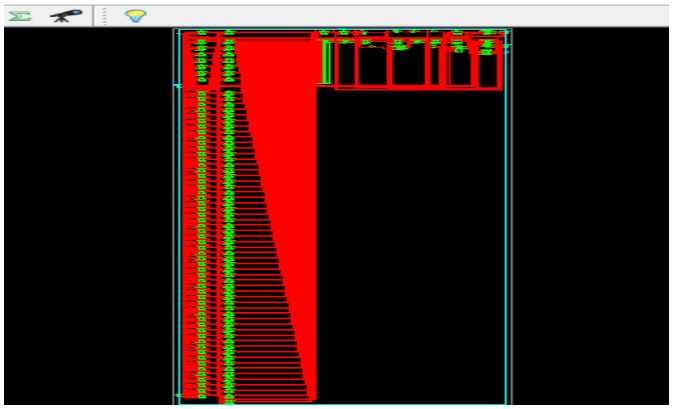


Figure 8.RTL Schematic of filter

5. SYNTHESIS REPORT

1.Advanced HDL Synthesis Report

Macro Statistics

# RAMs	: 1
64x16-bit dual-port distributed RAM	: 1
# Multipliers	: 1
16x10-bitregistered multiplier	: 1
# Counters	: 2
6-bit up counter	: 2
# Accumulators	: 1
30-bit up loadable accumulator	: 1
# Registers	: 1392
Flip-Flops	: 1392
# Multiplexers	: 3
10-bit 64-to-1 multiplexer	: 1
16-bit 2-to-1 multiplexer	: 1
30-bit 2-to-1 multiplexer	: 1

Power report

The .ncd file is shows the power consumed by different part of the system i.e.on chip power,clocks,DSPs,logic,signals,IOs etc.Using a Xilinx Power analyser the power is estimated as shown in figure 9.

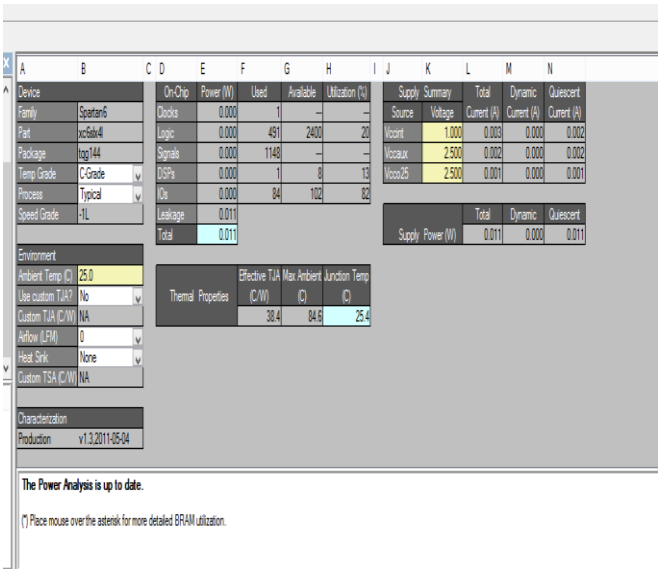


Figure 9:Xilinx Power Analyser

6. FUTURE SCOPE

In the Distributed arithmetic architecture shared-LUT design is proposed to realize DA computation.Dual port distributed RAM based LUTs are being used.DA decomposition for implementation of an FIR filter is the first thing to do.The proposed work also involves clock gating.

7. RESULTS AND CONCLUSION

The junction temperature found to be 25.10 C and the leakage power is 0.011W. On-Chip Power Summary is given in the table

7.1 On-Chip	Power (mW)	Used	Available	Utilization (%)
Clocks	0.40	1	---	---

Logic	0.00	491	2400	20
Signals	0.00	1148	---	---
IOs	0.00	84	102	82
DSPs	0.00	1	8	13
Static Power	10.97			
Total	11.36			

7.2. Thermal Summary

Effective TJA (C/W)	38.4
Max Ambient (C)	84.6
Junction Temp (C)	25.4

7.3. Power Supply Summary

	Total	Dynamic	Static Power
Supply Power (mW)	11.36	0.40	10.97

The HDL code generated is efficient The study of FIR filter design shows that it is linear phase and stable and therefore can be used in various applications to reduce the noise or can be used for waveshaping.

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